CLAIMS

1. Mode selector apparatus (FIG. 7) for automatically selecting one of a standard automatic switching mode and a soft automatic switching mode in a decision feedback equalizer (DFE), said mode selector apparatus being adapted for use in a data signal processing system with equalization, said mode selector apparatus comprising:

an equalizer (30) for providing first and second DFE outputs corresponding to a standard dd mode and a soft dd mode, respectively; and

a comparator (36) for comparing byte error rates (ByER) of said first and second DFE outputs for selecting as a superior mode that mode associated with a lower ByER and outputting the DFE output with said lower ByER.

2. Mode selector apparatus as recited in claim 1 wherein said standard automatic switching mode selectively exhibiting a blind mode and a standard decision directed (dd) mode and said soft automatic switching mode selectively exhibiting a blind mode and a soft dd mode.

3. Mode selector apparatus as recited in claim 2, including lock detector means (30) for providing a lock signal for indicating convergence of said DFE, said lock signal being derived from said DFE output signal with said lower BER.

4. Mode selector apparatus in accordance with claim 2, wherein said equalizer (30) for providing said first and second DFE output signals comprises decision feedback equalizer (DFE) means for processing said data signal and exhibiting concurrent soft and hard decision directed (dd) output signals.

5. Mode selector apparatus in accordance with claim 3, wherein said lock detector means (30) includes first and second lock detectors (30) for providing respective lock signals derived from respective ones of said DFE outputs.

6. Mode selector apparatus in accordance with claim 3, including a mode switch (38) for selectively placing said DFE outputs in one of

(a) one of said standard and soft dd modes and

(b) a blind mode, depending on said lock signal identifying convergence of said DFE.

7. Mode selector apparatus in accordance with claim 3, wherein a training mode replaces the blind mode and including a mode switch (38) for selectively placing said DFE outputs in one of

(a) one of said standard and soft dd modes and

(b) a training mode, depending on said lock signal identifying convergence of said DFE.

8. Mode selector apparatus in accordance with claim 1 further comprising:

a forward error correcting processor (32, 34) for processing said first and second DFE output signals by forward error correction (FEC) so as to provide respective first and second FEC output signals; wherein:

the comparator (36) determines which one of said standard automatic switching mode and said soft automatic switching mode is the superior mode in accordance with a defined comparison criterion, and outputs an output signal of said one superior mode.

9. Mode selector apparatus in accordance with claim 8, wherein said forward error correcting processor (32, 34) includes a trellis decoder (32, 34) and a Reed Solomon (RS) decoder (32, 34) .

10. Mode selector apparatus in accordance with claim 8, wherein said defined comparison criterion comprises said comparator (36) comparing uncorrectable segment rates (USR) out of said RS decoder, selecting as a

superior mode that mode associated with a lower USR and outputting the DFE output signal with said lower USR.

11. Mode selector apparatus in accordance with claim 8, wherein said defined comparison criterion comprises said comparator (36) comparing estimated bit error rate (BER) out of said RS decoder, selecting as a superior mode that mode associated with a lower BER and outputting the DFE output signal with said lower BER.

12. Mode selector apparatus in accordance with claim 1, wherein said equalizer for providing first and second DFE output signals includes equalizer filtering means and slicer means (30) coupled to said mode switch (38) for providing said first and second DFE output signals.

13. Mode selector apparatus in accordance with claim 8, wherein said forward error correcting processor comprises parallel processing means (32, 34) for respectively providing said first and second FEC output signals.

14. Apparatus in accordance with claim 5, including a mode switch coupled to said first and second DFE output signals, said respective lock output signals, and to said comparison signal for monitoring said comparison signal for

selecting one of said respective lock output signals to provide said lock signal, depending upon said comparison signal.

15. Apparatus in accordance with claim 14, wherein said mode switch (38) selects one of said respective lock output signals corresponding to said superior mode.

16. A method for automatically selecting one of a standard automatic switching mode and a soft automatic switching mode in a decision feedback equalizer (DFE) for receiving a data signal, said method comprising the steps of:

processing a received signal, including equalization and forward error correction (FEC);

providing first and second DFE output signals corresponding to said standard automatic switching mode and said soft automatic switching mode, respectively;

processing said first and second DFE output signals so as to provide respective first and second FEC output signals;

comparing byte error rate (ByER) in each of said first and second FEC output signals to ascertain which of said automatic switching mode and said soft automatic switching mode is the superior mode for ByER under given conditions;

deriving a selection signal from said superior mode; and

utilizing said selection signal for controlling said DFE.

17. A method in accordance with claim 16, wherein said step of utilizing said selection signal for controlling said DFE comprises a step of setting said DFE into one of

(a) a blind mode, and

(b) one of a standard decision directed mode and a soft decision directed mode, depending on said selection signal.

18. A method in accordance with claim 17, wherein said step for providing first and second DFE output signals includes:

a step of equalizer filtering; and

a step of signal slicing coupled for providing said first and second DFE output signals.

19. A method in accordance with claim 17, wherein said step of processing said first and second DFE output signals comprises a step of

processing said first and second DFE output signals in parallel paths for respectively providing said first and second FEC output signals.

20. A method in accordance with claim 17, wherein said step of FEC processing includes steps of trellis decoding and Reed Solomon decoding.

21. A method in accordance with claim 16, wherein said step of utilizing said selection signal for controlling said DFE comprises:

deriving a first lock signal from said first FEC output signal;

deriving a second lock signal from said second FEC output signal; and

selecting one of said first and second lock signals for controlling said DFE, depending on said selection signal.

22. A method in accordance with claim 19, wherein said step of processing said first and second DFE output signals comprises a step of processing said data signal by a decision feedback equalizer (DFE) exhibiting concurrent soft and hard decision directed (dd) operating modes for providing said first and second DFE output signals.

23. A method in accordance with claim 22, including providing concurrently in each output symbol soft decision bit representation concurrently both hard and soft decision representations.

24. A method in accordance with claim 16, wherein said step of utilizing said selection signal for controlling said DFE comprises:

deriving a lock signal from one of said first and second FEC output signal, depending on said selection signal; and

utilizing said lock signal for controlling said DFE.

25. A method in accordance with claim 16, wherein said step of utilizing said selection signal for controlling said DFE comprises:

deriving said lock signal from that one of said first and second FEC output signal associated with said superior mode.